Amendments to the Specification

The specification has been amended as set forth below to correct for certain informalities. No new matter has been added.

First paragraph to begin on page 1:

> Programmable Switching [[AC]] Current Booster for Faster Edge-Rate Output in High Speed Applications

Second paragraph to begin on page 2:

> In order to achieve successful operation in circuits operating at high speeds, typically greater than 200Mhz at present, existing I/O signaling standards require a signal waveform having fast edge rate and small output voltage swing, in order to maintain precise phase relationships between the high frequency signals. These two crucial requirements, fast edge rate and small output voltage swing, are physical characteristics inherently in opposition with each other. Overdriving for a faster edge rate directly results in increased output voltage swing. It is therefore becoming increasingly difficult to meet both requirements when the same output current settings are used for both [[AC]]switching and [[DC]]holding states as circuit speeds continue to increase.

Last paragraph to begin on page 2:

> [[An AC]]A switching current booster is described herein capable of operating at high frequencies for high speed applications and is described in several embodiments including a single-ended output circuit and a differential output circuit. Although the signal frequencies are typically around 200MHz in one embodiment, the present invention may be equally applicable to circuit speeds that are lower or higher. Embodiments of the present invention can be programmed to provide any specific combination of output current, capacitive loading, output voltage swing and signal edge rate (typically in the order of 100 picoseconds) in order to conform to any one of several well known I/O signaling standards.

Last paragraph to begin on page 3:

Embodiments of the present invention allow for bifurcated control of the [[AC]] switching rate and the [[DC]]holding state of a given output signal, in order to achieve faster rising and falling edge rates without the undesirable increased output voltage swing. Fast edge rates require a large switching current to charge up the capacitive loading, while providing a small [[DC]]holding current to limit the output voltage swing. The programmable current booster described here provides a separate [[AC]]switching current during the output switching phase, while not affecting the [[DC]]holding current or the output voltage swing. Importantly, the strength and the duration of the [[AC]]switching booster current are programmable to allow a user the maximum flexibility in conforming to any of the I/O signaling standards such as HSTL, SSTL, LVDS, LVPECL or HyperTransport, though the present invention is not limited to only those standards. Embodiments of the present invention may be equally applicable to other relevant existing standards as well as those standards which have yet to be proposed or fully developed.

Last paragraph to begin on page 4:

FIG. 2B illustrates a timing diagram of the single-ended output driver operation in the case with the [[DC]]holding output enabled.

First paragraph to begin on page 5:

FIG. 2C illustrates a timing diagram of the single-ended output driver operation in the case with the [[AC]]switching current booster enabled.

Third paragraph to begin on page 5:

FIG. 4 shows exemplary details of the differential [[DC]]holding stage rising edge control circuit.

Fourth paragraph to begin on page 5:

FIG. 5 shows exemplary details of the differential [[DC]]holding stage falling edge control circuit.

Last paragraph to begin on page 6:

> Output transistors 220 and 224 are used to regulate the magnitude of the [[AC]]switching current and [[DC]]holding current. Transistor 220 is controlled by the output of OR gate 212. Transistor 224 is controlled by the output of AND gate 216. The duration of the current flowing through the output transistors is programmable via the rising edge control circuit 106 and falling edge control circuit 110.

Second paragraph to begin on page 7:

> If configuration signal 104 is LOW, output transistor 220 is always off. When configuration signal 104 is HIGH, output transistor 220 is enabled, but the duration of its ON state is programmable in two ways. First, if RAM bit 202 is programmed to be HIGH, then output transistor 220 will remain ON as long as common input signal 102 is HIGH, thereby providing a continuous [[DC]]holding output current which would contribute to the output voltage swing. Second, if RAM bit 202 is configured to be LOW, then output transistor 220 will be ON only during the edge transition time when input signal 102 is switching from LOW to HIGH. The duration of this ON time is programmable via programmable delay element 206. This short period of current through output transistor 220 will charge up the loading on output pin 114, and reduce the rise time, but will not affect the [[DC]]holding output voltage swing.

Last paragraph to begin on page 7:

> Similarly, output transistor 224 can be totally disabled when configuration signal 103 is LOW, or can be programmed to be ON as long as common input signal 102 is low, or can even be programmed to be ON only when common input signal 102 is switching from HIGH to LOW, thereby providing a [[DC]]holding output current. Configuration bit 204 controls operation of falling edge circuit 110. Programmable delay element 208 is similarly used to control the ON duration of output transistor 224.

Last paragraph to begin on page 8:

Additional parallel-coupled sets of control circuits can be connected in the cascaded manner shown for at least a second set of rising and falling edge circuitry 236, each such output set having varying channel width, thereby allowing users to program them into various combinations of [[DC]]holding and [[AC]]switching current paths. To control the strength of the current for the output signal 114, several output transistors may be connected in parallel. In this case, pull-up output transistors 220 and 232 are shown connected in parallel, and so are pull-down output transistors 224 and 234. At least one of pull-up output transistors 220 and 232 and one of pull-down output transistors 224 and 234 should be programmed to provide [[DC]]holding current. In this manner, users can select different strengths for the [[DC]]holding and [[AC]]switching currents separately, thereby achieving a fast edge rate with a relatively small output voltage swing.

First paragraph to begin on page 9:

Figure 2B is a timing diagram for an exemplary operational case of the circuit 100 of Figure 2A. Refer to both Figure 2A and Figure 2B. In this exemplary case, the [[DC]]holding output is enabled. In this case, the configuration bit 202 (Figure 2A) is high; configuration bit 204 is low; enable 104 is high; enable 103 is high; the C and D inputs of OR gate 212 are low and the F input of AND gate 216 is high. Waveform 251 represents transitions on the input 102. Waveform 252 represents transitions on the output of the inverter circuit coupled to receive input 102. Waveform 253 represents transitions on the input to output transistor 220. Waveform 254 represents transitions on the output transistor 224. Waveform 255 represents transitions on the output 114.

Third paragraph to begin on page 9:

According to this operational mode, if configuration bit 202 is programmed high, then transistor 220 will be on as long as the input signal 102 is high, providing a continuous output current which would contribute to the [[DC]]holding output voltage swing.

Last paragraph to begin on page 9:

Figure 2C is a timing diagram of the [[AC]]switching booster control rising edge circuit 106 for an exemplary operational case of the circuit 100 of Figure 2A. Refer to both Figure 2A and Figure 2C. In this exemplary case, the [[AC]]switching booster control circuit 106 is enabled while output transistors 232 and 234 are programmed to provide [[DC]]holding output current. In this case, the configuration bit 202 (Figure 2A) is low; configuration bit 204 is high; enable 104 is high; enable 103 is high; and the D input of OR gate 212 is low. Waveform 256 represents input B of NOR gate 210. Waveform 257 represents input C of OR gate 212. Waveform 258 represents input E of NAND gate 214. Waveform 259 represents input F of AND gate 216. Waveforms 251-255 are analogous to those circuit points as described with reference to Figure 2B.

Second paragraph to begin on page 10:

In operation, if bit 202 is low, then transistor 220 will be ON only during the transition time when the input 102 is switching from low to high; the duration of this ON time can be programmed by the programmable delay element 206. This short period of current through transistor 220 will charge up the loading on the output pin and reduce the rise time, but will not generally affect the [[DC]]holding output voltage swing.

Third paragraph to begin on page 10:

Similarly, transistor 224 can be totally disabled when enable 103 is low, or programmed to provide a [[DC]]holding output current if enable 103 is high and 204 is low, or further, programmed to be ON only when the input is switching from high to low. The programmable delay 208 controls the duration of the ON state.

First paragraph to begin on page 11:

FIG. 3 is a preferred implementation of a differential output driver 700 according to one embodiment of the present invention. Output transistors 516, 518, 528 and 530 provide [[DC]]holding output current, while output transistors 522, 523, 520 and 521 are [[AC]]switching current boosters. [[DC]]holding stage rising edge control circuits 510 have

the analogous delay as the [[AC]]switching booster control circuits 106, so the [[DC]]holding and [[AC]]switching currents are switched on simultaneously. The control circuits 106 for current-regulating output transistors 520 and 522 in this differential embodiment are identical to that of circuit 106 for the single-ended case of FIG. 2A. Similarly, control circuits 110 for output transistors 521 and 523 are identical to that of circuit 110 for the single-ended case of FIG. 2A.

Last paragraph to begin on page 11:

FIG. 4 shows exemplary details of a preferred circuit implementation of the differential [[DC]]holding stage rising edge control circuit 510 for the differential embodiment 700 of Figure 3. The OR gate 602 has a first OR input from the common input or data signal 502/504 received from the integrated circuit device, a second OR input from an input/ output configuration signal 514 ("enable signal") received from the integrated circuit device and inverted via an inverter circuit, and a third OR input coupled to the second OR input (e.g., also from the output of the inverter circuit). Output transistor 516/518 of Fig. 3 is coupled to the output of OR gate 602.

Second paragraph to begin on page 12:

The [[DC]]holding stage rising edge control circuits 510 should be designed to have the same delay as the rising edge [[AC]]switching booster control circuits 106, so the [[DC]]holding and [[AC]]switching currents are switched on simultaneously. Alternately, rising edge control circuit 106 can be used to control output transistors 516/ 518, again providing simultaneous switching on for the [[DC]]holding and [[AC]]switching currents.

Last paragraph to begin on page 12:

FIG. 5 shows exemplary details of a preferred circuit implementation of the differential [[DC]]holding stage falling edge control circuit 512 for the differential embodiment 700 of Figure 3. The AND gate 702 is coupled to receive a first AND input from the common input signal 502/504 received from the integrated circuit device, a second AND input from an input/output configuration signal 514 ("enable signal") received from the integrated circuit

device, and a third AND input coupled to the second AND input. Output transistor 528/530 are coupled to receive the output of AND gate 702.

Second paragraph to begin on page 13:

The [[DC]]holding stage falling edge control circuit 512 should be designed to have the same delay as the [[AC]]switching booster control circuits 110, so the [[DC]]holding and [[AC]]switching currents are switched on simultaneously. Or alternately, falling edge control circuit 110 can be used to control output transistors 528 and 530, whereby the [[DC]]holding and [[AC]]switching currents will be switched on simultaneously.

Last paragraph to begin on page 13:

Figure 6 is a timing diagram for an exemplary operational case of the circuit 700 of Figure 3. Refer to both Figure 3 and Figure 6. In this case, enable 532, enable 534 and enable 514 are all high; input 202 (of [[AC]]switching booster control block 106) is low and configuration bit 204 (of falling edge control block 110) is high. Waveform 610 represents input 502. Waveform 615 represents the output of the inverter that receives input 502. Waveform 620 represents input 504. Waveform 625 represents the output of the inverter that receives input 504. Waveform 630 represents the gate signal at output transistors 516 and 528. Waveform 635 represents the gate signal at output transistors 518 and 530. Waveform 640 represents the gate signal for transistor 522. Waveform 645 represents the gate signal for transistor 523. Waveform 650 represents the gate signal for transistor 520. Waveform 655 represents the gate signal for transistor 521. Waveforms 660 and 665 represent the differential output signals 506 and 508, respectively.

First paragraph to begin on page 14:

In operation, output transistors 516, 528, 518 and 530 provide [[DC]]holding output current, while transistors 522, 523, 520 and 521 are [[AC]]switching current boosters. The control circuits 510 and 512 for the [[DC]]holding output transistors are designed to have the same delay as the [[AC]]switching booster control circuits 106 and 110, so the [[DC]]holding current and [[AC]]switching current will be switched on at the same time.

Second paragraph to begin on page 14:

While specific circuits have been used to describe the present invention, the idea of using a programmable current booster in an integrated circuit output driver, with programmable duration and programmable strength of the [[AC]]switching booster current may be implemented using other circuit embodiments. It is intended that the invention not be limited to the particular embodiments disclosed, but that the invention will include all embodiments and all equivalents falling within the scope of the claims.